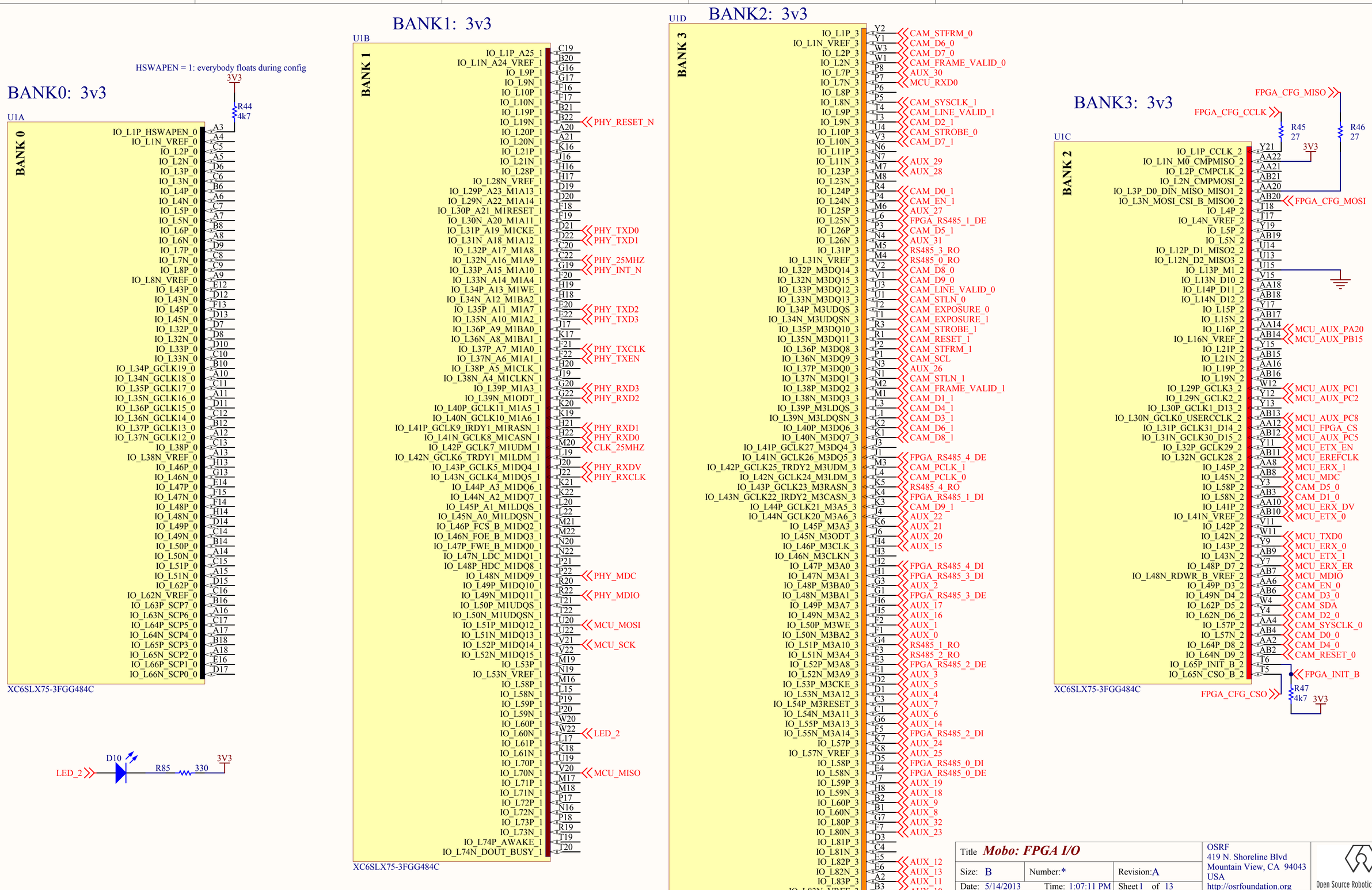
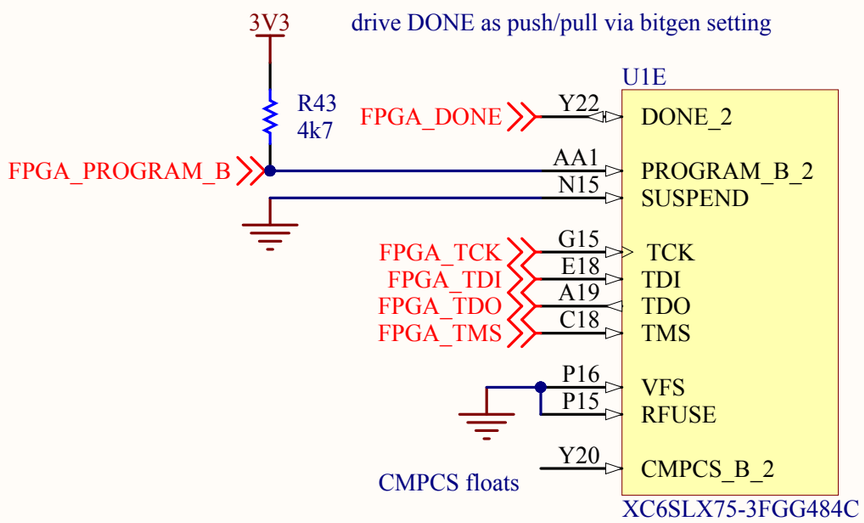
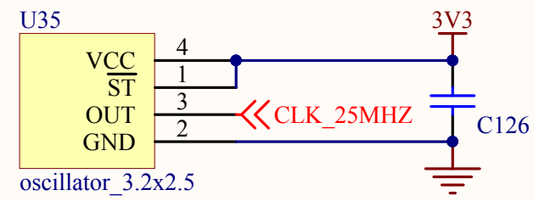
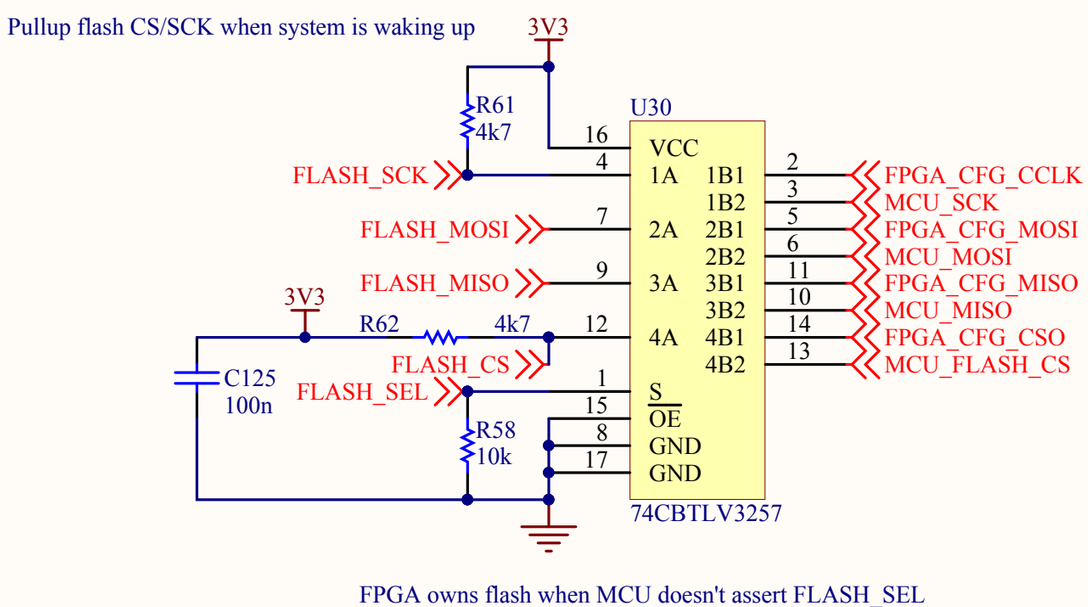

BANK0: 3v3
U1A
BANK 0
HSWAPEN = 1: everybody floats during config
3V3
R44
4k7
IO_L1P_HSWAPEN_0 A3
IO_L1N_VREF_0 A4
IO_L2P_0 C5
IO_L2N_0 A5
IO_L3P_0 D6
IO_L3N_0 C6
IO_L4P_0 B6
IO_L4N_0 A6
IO_L5P_0 C7
IO_L5N_0 A7
IO_L6P_0 B8
IO_L6N_0 A8
IO_L7P_0 D9
IO_L7N_0 C8
IO_L8P_0 C9
IO_L8N_VREF_0 A9
IO_L43P_0 E12
IO_L43N_0 D12
IO_L45P_0 F13
IO_L45N_0 D13
IO_L32P_0 D7
IO_L32N_0 D8
IO_L33P_0 D10
IO_L33N_0 C10
IO_L34P_GCLK19_0 B10
IO_L34N_GCLK18_0 A10
IO_L35P_GCLK17_0 C11
IO_L35N_GCLK16_0 A11
IO_L36P_GCLK15_0 D11
IO_L36N_GCLK14_0 C12
IO_L37P_GCLK13_0 B12
IO_L37N_GCLK12_0 A12
IO_L38P_0 C13
IO_L38N_VREF_0 A13
IO_L46P_0 H13
IO_L46N_0 G13
IO_L47P_0 E14
IO_L47N_0 F15
IO_L48P_0 F14
IO_L48N_0 H14
IO_L49P_0 D14
IO_L49N_0 C14
IO_L50P_0 B14
IO_L50N_0 A14
IO_L51P_0 C15
IO_L51N_0 A15
IO_L62P_0 D15
IO_L62N_VREF_0 C16
IO_L63P_SCP7_0 B16
IO_L63N_SCP6_0 A16
IO_L64P_SCP5_0 C17
IO_L64N_SCP4_0 A17
IO_L65P_SCP3_0 B18
IO_L65N_SCP2_0 A18
IO_L66P_SCP1_0 E16
IO_L66N_SCP0_0 D17
XC6SLX75-3FGG484C
BANK1: 3v3
U1B
BANK 1
IO_L1P_A25_1 C19
IO_L1N_A24_VREF_1 B20
IO_L9P_1 G16
IO_L9N_1 G17
IO_L10P_1 F16
IO_L10N_1 F17
IO_L19P_1 B21
IO_L19N_1 B22 PHY_RESET_N
IO_L20P_1 A20
IO_L20N_1 A21
IO_L21P_1 K16
IO_L21N_1 J16
IO_L28P_1 H16
IO_L28N_VREF_1 H17
IO_L29P_A23_M1A13_1 D19
IO_L29N_A22_M1A14_1 D20
IO_L30P_A21_M1RESET_1 F18
IO_L30N_A20_M1A11_1 F19
IO_L31P_A19_M1CKE_1 D21 PHY_TXD0
IO_L31N_A18_M1A12_1 D22 PHY_TXD1
IO_L32P_A17_M1A8_1 C20
IO_L32N_A16_M1A9_1 C22 PHY_25MHZ
IO_L33P_A15_M1A10_1 G19 PHY_INT_N
IO_L33N_A14_M1A4_1 F20
IO_L34P_A13_M1WE_1 H19
IO_L34N_A12_M1BA2_1 H18
IO_L35P_A11_M1A7_1 E20 PHY_TXD2
IO_L35N_A10_M1A2_1 E22 PHY_TXD3
IO_L36P_A9_M1BA0_1 J17
IO_L36N_A8_M1BA1_1 K17
IO_L37P_A7_M1A0_1 F21 PHY_TXCLK
IO_L37N_A6_M1A1_1 F22 PHY_TXEN
IO_L38P_A5_M1CLK_1 H20
IO_L38N_A4_M1CLKN_1 J19
IO_L39P_M1A3_1 G20 PHY_RXD3
IO_L39N_M1ODT_1 G22 PHY_RXD2
IO_L40P_GCLK11_M1A5_1 K20
IO_L40N_GCLK10_M1A6_1 K19
IO_L41P_GCLK9_IRDY1_M1RASN_1 H21 PHY_RXD1
IO_L41N_GCLK8_M1CASN_1 H22 PHY_RXD0
IO_L42P_GCLK7_M1UDM_1 M20 CLK_25MHZ
IO_L42N_GCLK6_TRDY1_M1LDM_1 L19
IO_L43P_GCLK5_M1DQ4_1 J20 PHY_RXDV
IO_L43N_GCLK4_M1DQ5_1 J22 PHY_RXCLK
IO_L44P_A3_M1DQ6_1 K21
IO_L44N_A2_M1DQ7_1 K22
IO_L45P_A1_M1LDQS_1 L20
IO_L45N_A0_M1LDQSN_1 L22
IO_L46P_FCS_B_M1DQ2_1 M21
IO_L46N_FOE_B_M1DQ3_1 M22
IO_L47P_FWE_B_M1DQ0_1 N20
IO_L47N_LDC_M1DQ1_1 N22
IO_L48P_HDC_M1DQ8_1 P21
IO_L48N_M1DQ9_1 P22 PHY_MDC
IO_L49P_M1DQ10_1 R20
IO_L49N_M1DQ11_1 R22 PHY_MDIO
IO_L50P_M1UDQS_1 T21
IO_L50N_M1UDQSN_1 T22
IO_L51P_M1DQ12_1 U20 MCU_MOSI
IO_L51N_M1DQ13_1 U22
IO_L52P_M1DQ14_1 V21 MCU_SCK
IO_L52N_M1DQ15_1 V22
IO_L53P_1 M19
IO_L53N_VREF_1 N19
IO_L58P_1 M16
IO_L58N_1 L15
IO_L59P_1 P19
IO_L59N_1 P20
IO_L60P_1 W20
IO_L60N_1 W22 LED_2
IO_L61P_1 L17
IO_L61N_1 K18
IO_L70P_1 U19
IO_L70N_1 V20 MCU_MISO
IO_L71P_1 M17
IO_L71N_1 M18
IO_L72P_1 P17
IO_L72N_1 N16
IO_L73P_1 P18
IO_L73N_1 R19
IO_L74P_AWAKE_1 T19
IO_L74N_DOUT_BUSY_1 T20
XC6SLX75-3FGG484C
BANK2: 3v3
U1D
BANK 3
IO_L1P_3 Y2 CAM_STFRM_0
IO_L1N_VREF_3 Y1 CAM_D6_0
IO_L2P_3 W3 CAM_D7_0
IO_L2N_3 W1 CAM_FRAME_VALID_0
IO_L7P_3 P8 AUX_30
IO_L7N_3 P7 MCU_RXD0
IO_L8P_3 P6
IO_L8N_3 P5 CAM_SYSCLK_1
IO_L9P_3 T4 CAM_LINE_VALID_1
IO_L9N_3 T3 CAM_D2_1
IO_L10P_3 U4 CAM_STROBE_0
IO_L10N_3 V3 CAM_D7_1
IO_L11P_3 N6
IO_L11N_3 N7 AUX_29
IO_L23P_3 M7 AUX_28
IO_L23N_3 M8
IO_L24P_3 R4 CAM_D0_1
IO_L24N_3 P4 CAM_EN_1
IO_L25P_3 M6 AUX_27
IO_L25N_3 L6 FPGA_RS485_1_DE
IO_L26P_3 P3 CAM_D5_1
IO_L26N_3 N4 AUX_31
IO_L31P_3 M5 RS485_3_RO
IO_L31N_VREF_3 M4 RS485_0_RO
IO_L32P_M3DQ14_3 V2 CAM_D8_0
IO_L32N_M3DQ15_3 V1 CAM_D9_0
IO_L33P_M3DQ12_3 U3 CAM_LINE_VALID_0
IO_L33N_M3DQ13_3 U1 CAM_STLN_0
IO_L34P_M3UDQS_3 T2 CAM_EXPOSURE_0
IO_L34N_M3UDQSN_3 T1 CAM_EXPOSURE_1
IO_L35P_M3DQ10_3 R3 CAM_STROBE_1
IO_L35N_M3DQ11_3 R1 CAM_RESET_1
IO_L36P_M3DQ8_3 P2 CAM_STFRM_1
IO_L36N_M3DQ9_3 P1 CAM_SCL
IO_L37P_M3DQ0_3 N3 AUX_26
IO_L37N_M3DQ1_3 N1 CAM_STLN_1
IO_L38P_M3DQ2_3 M2 CAM_FRAME_VALID_1
IO_L38N_M3DQ3_3 M1 CAM_D1_1
IO_L39P_M3LDQS_3 L3 CAM_D4_1
IO_L39N_M3LDQSN_3 L1 CAM_D3_1
IO_L40P_M3DQ6_3 K2 CAM_D6_1
IO_L40N_M3DQ7_3 K1 CAM_D8_1
IO_L41P_GCLK27_M3DQ4_3 J3
IO_L41N_GCLK26_M3DQ5_3 J1 FPGA_RS485_4_DE
IO_L42P_GCLK25_TRDY2_M3UDM_3 M3 CAM_PCLK_1
IO_L42N_GCLK24_M3LDM_3 L4 CAM_PCLK_0
IO_L43P_GCLK23_M3RASN_3 K5 RS485_4_RO
IO_L43N_GCLK22_IRDY2_M3CASN_3 K4 FPGA_RS485_1_DI
IO_L44P_GCLK21_M3A5_3 K3 CAM_D9_1
IO_L44N_GCLK20_M3A6_3 J4 AUX_22
IO_L45P_M3A3_3 K6 AUX_21
IO_L45N_M3ODT_3 J6 AUX_20
IO_L46P_M3CLK_3 H4 AUX_15
IO_L46N_M3CLKN_3 H3
IO_L47P_M3A0_3 H2 FPGA_RS485_4_DI
IO_L47N_M3A1_3 H1 FPGA_RS485_3_DI
IO_L48P_M3BA0_3 G3 AUX_2
IO_L48N_M3BA1_3 G1 FPGA_RS485_3_DE
IO_L49P_M3A7_3 H6 AUX_17
IO_L49N_M3A2_3 H5 AUX_16
IO_L50P_M3WE_3 F2 AUX_1
IO_L50N_M3BA2_3 F1 AUX_0
IO_L51P_M3A10_3 G4 RS485_1_RO
IO_L51N_M3A4_3 F3 RS485_2_RO
IO_L52P_M3A8_3 E3 FPGA_RS485_2_DE
IO_L52N_M3A9_3 E1 AUX_3
IO_L53P_M3CKE_3 D2 AUX_5
IO_L53N_M3A12_3 D1 AUX_4
IO_L54P_M3RESET_3 C3 AUX_7
IO_L54N_M3A11_3 C1 AUX_6
IO_L55P_M3A13_3 G6 AUX_14
IO_L55N_M3A14_3 F5 FPGA_RS485_2_DI
IO_L57P_3 K7 AUX_24
IO_L57N_VREF_3 K8 AUX_25
IO_L58P_3 D5 FPGA_RS485_0_DI
IO_L58N_3 E4 FPGA_RS485_0_DE
IO_L59P_3 J7 AUX_19
IO_L59N_3 H8 AUX_18
IO_L60P_3 B2 AUX_9
IO_L60N_3 B1 AUX_8
IO_L80P_3 G7 AUX_32
IO_L80N_3 F7 AUX_23
IO_L81P_3 D3
IO_L81N_3 C4
IO_L82P_3 E5 AUX_12
IO_L82N_3 E6 AUX_13
IO_L83P_3 A2 AUX_11
IO_L83N_VREF_3 B3 AUX_10
XC6SLX75-3FGG484C
BANK3: 3v3
U1C
BANK 2
FPGA_CFG_MISO
FPGA_CFG_CCLK
R45
27
R46
27
3V3
IO_L1P_CCLK_2 Y21
IO_L1N_M0_CMPMISO_2 AA22
IO_L2P_CMPCLK_2 AA21
IO_L2N_CMPMOSI_2 AB21
IO_L3P_D0_DIN_MISO_MISO1_2 AA20
IO_L3N_MOSI_CSI_B_MISO0_2 AB20 FPGA_CFG_MOSI
IO_L4P_2 T18
IO_L4N_VREF_2 T17
IO_L5P_2 Y19
IO_L5N_2 AB19
IO_L12P_D1_MISO2_2 U14
IO_L12N_D2_MISO3_2 U13
IO_L13P_M1_2 U15
IO_L13N_D10_2 V15
IO_L14P_D11_2 AA18
IO_L14N_D12_2 AB18
IO_L15P_2 Y17
IO_L15N_2 AB17
IO_L16P_2 AA14 MCU_AUX_PA20
IO_L16N_VREF_2 AB14 MCU_AUX_PB15
IO_L21P_2 Y15
IO_L21N_2 AB15
IO_L19P_2 AA16
IO_L19N_2 AB16
IO_L29P_GCLK3_2 W12
IO_L29N_GCLK2_2 Y12 MCU_AUX_PC1
IO_L30P_GCLK1_D13_2 Y13 MCU_AUX_PC2
IO_L30N_GCLK0_USERCCLK_2 AB13
IO_L31P_GCLK31_D14_2 AA12 MCU_AUX_PC8
IO_L31N_GCLK30_D15_2 AB12 MCU_FPGA_CS
IO_L32P_GCLK29_2 Y11 MCU_AUX_PC5
IO_L32N_GCLK28_2 AB11 MCU_ETX_EN
IO_L45P_2 AA8 MCU_EREFCLK
IO_L45N_2 AB8 MCU_ERX_1
IO_L58P_2 Y3 MCU_MDC
IO_L58N_2 AB3 CAM_D5_0
IO_L41P_2 AA10 CAM_D1_0
IO_L41N_VREF_2 AB10 MCU_ERX_DV
IO_L42P_2 V11 MCU_ETX_0
IO_L42N_2 W11
IO_L43P_2 Y9 MCU_TXD0
IO_L43N_2 AB9 MCU_ERX_0
IO_L48P_D7_2 Y7 MCU_ETX_1
IO_L48N_RDWR_B_VREF_2 AB7 MCU_ERX_ER
IO_L49P_D3_2 AA6 MCU_MDIO
IO_L49N_D4_2 AB6 CAM_EN_0
IO_L62P_D5_2 W4 CAM_D3_0
IO_L62N_D6_2 Y4 CAM_SDA
IO_L57P_2 AA4 CAM_D2_0
IO_L57N_2 AB4 CAM_SYSCLK_0
IO_L64P_D8_2 AA2 CAM_D0_0
IO_L64N_D9_2 AB2 CAM_D4_0
IO_L65P_INIT_B_2 T6 CAM_RESET_0
IO_L65N_CSO_B_2 T5 FPGA_INIT_B
XC6SLX75-3FGG484C
FPGA_CFG_CSO
R47
4k7
3V3
D10
LED_2
R85
330
3V3
Title Mobo: FPGA I/O
Size: B
Number:*
Revision:A
Date: 5/14/2013
Time: 1:07:11 PM
Sheet 1 of 13
Designer: Morgan Quigley
OSRF
419 N. Shoreline Blvd
Mountain View, CA 94043
USA
http://osrfoundation.org
Open Source Robotics Foundation



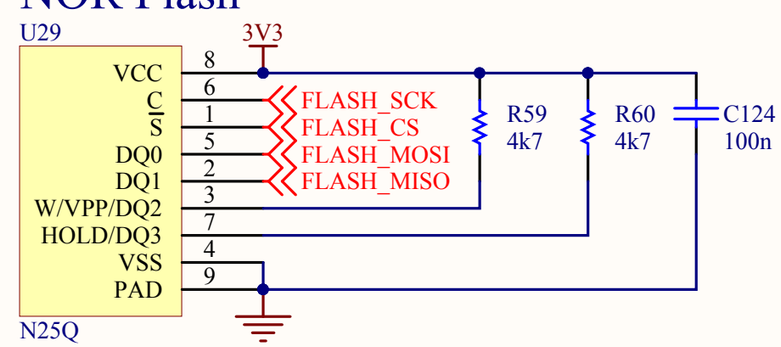
25 MHz clock



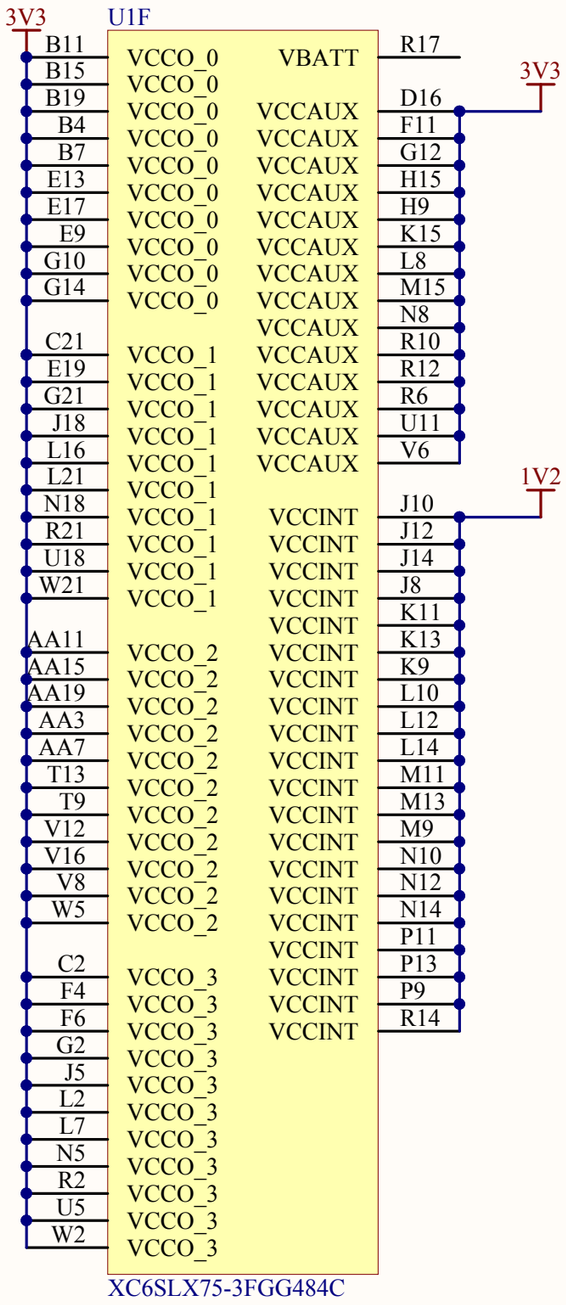
0201 jumpers which put the FPGA onto the external JTAG chain

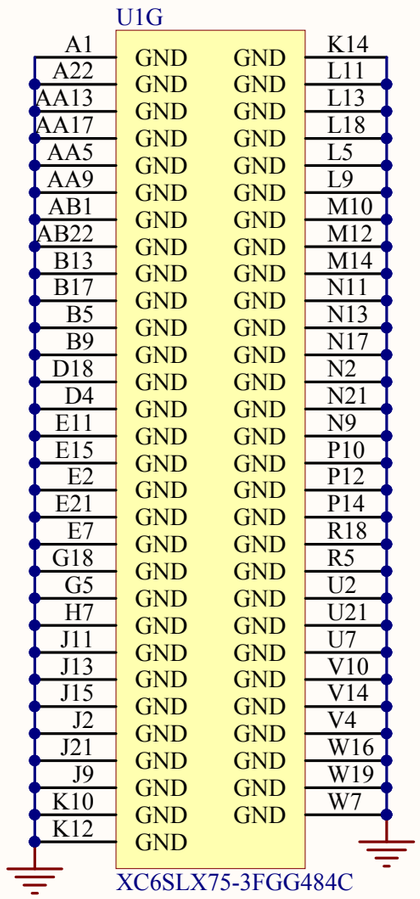


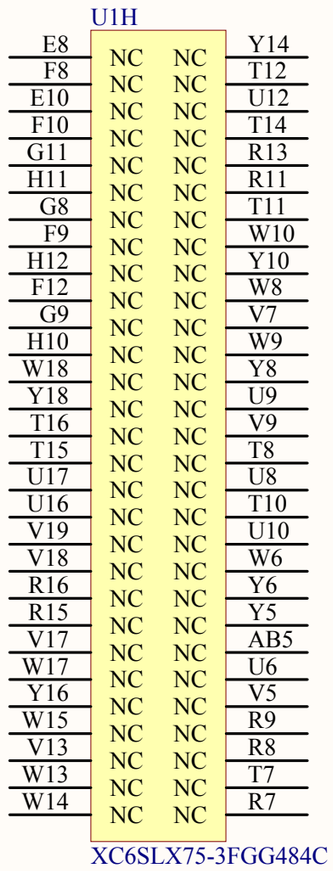
NOR Flash



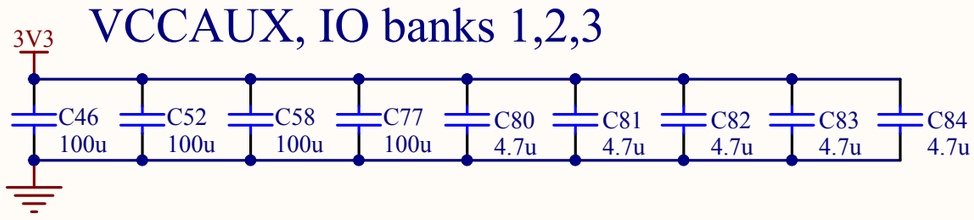
Title *Mobo: FPGA Configuration*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org Open Source Robotics Foundation
Size: A	Number:*	Revision:A	
Date: 5/14/2013	Time: 1:07:11 PM	Sheet 2 of 13	
Designer: Morgan Quigley			

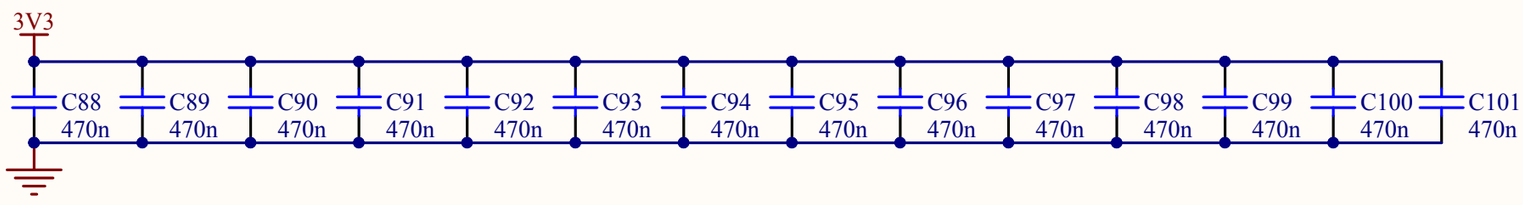




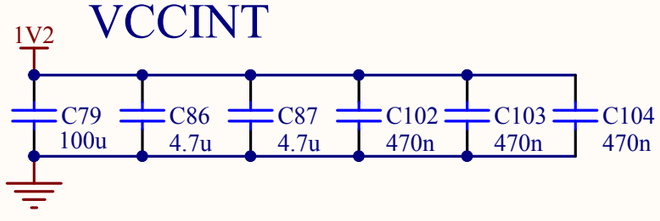


VCCAUX, IO banks 1,2,3

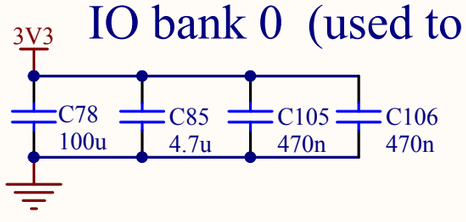




VCCINT



IO bank 0 (used to be 1.8v, not anymore)



capacitor quantities from Xilinx design guide: UG393

Title *Mobo: FPGA Power*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:*	Revision:A	
Date: 5/14/2013	Time: 1:07:11 PM	Sheet 3 of 13	
Designer: Morgan Quigley			

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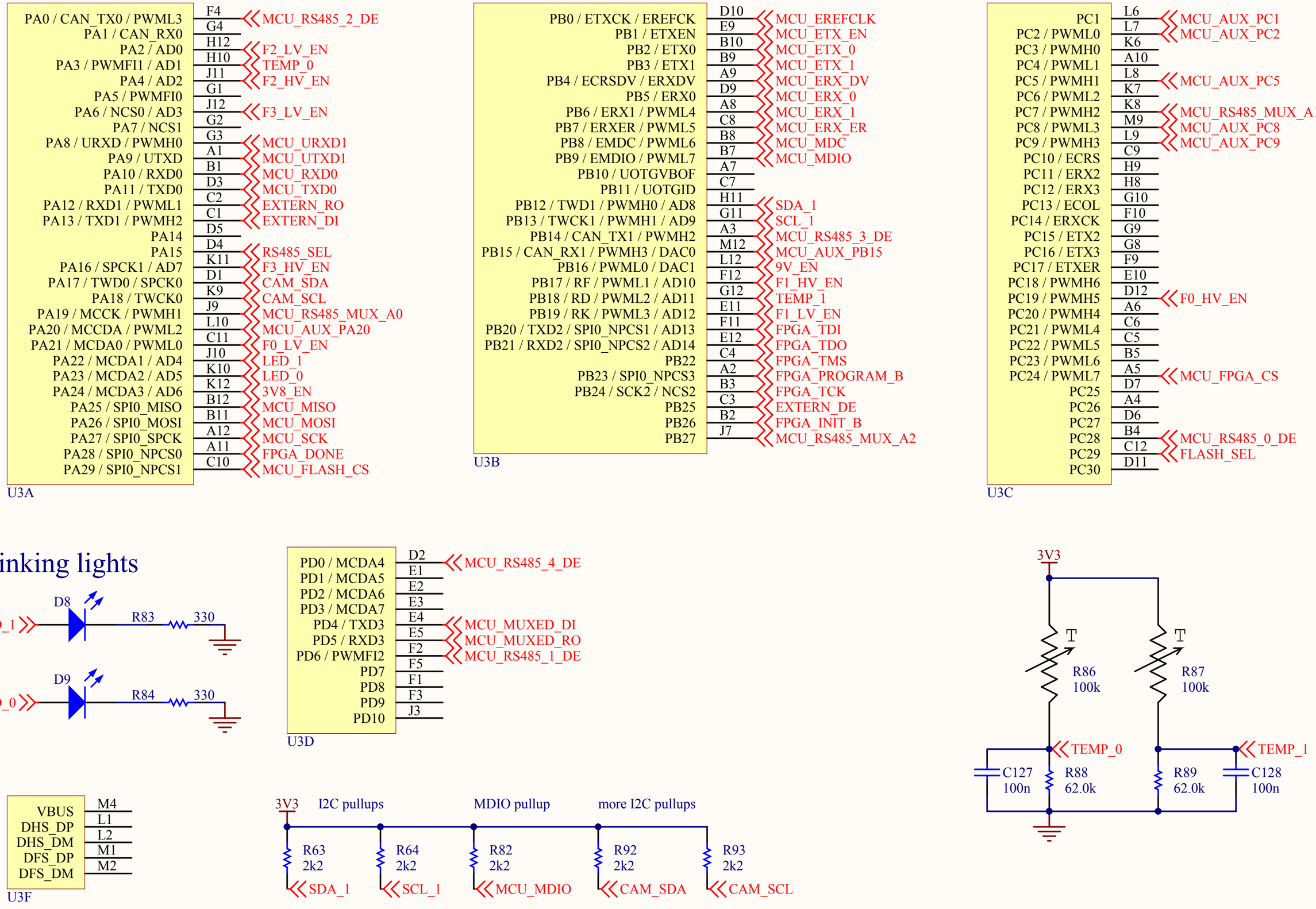
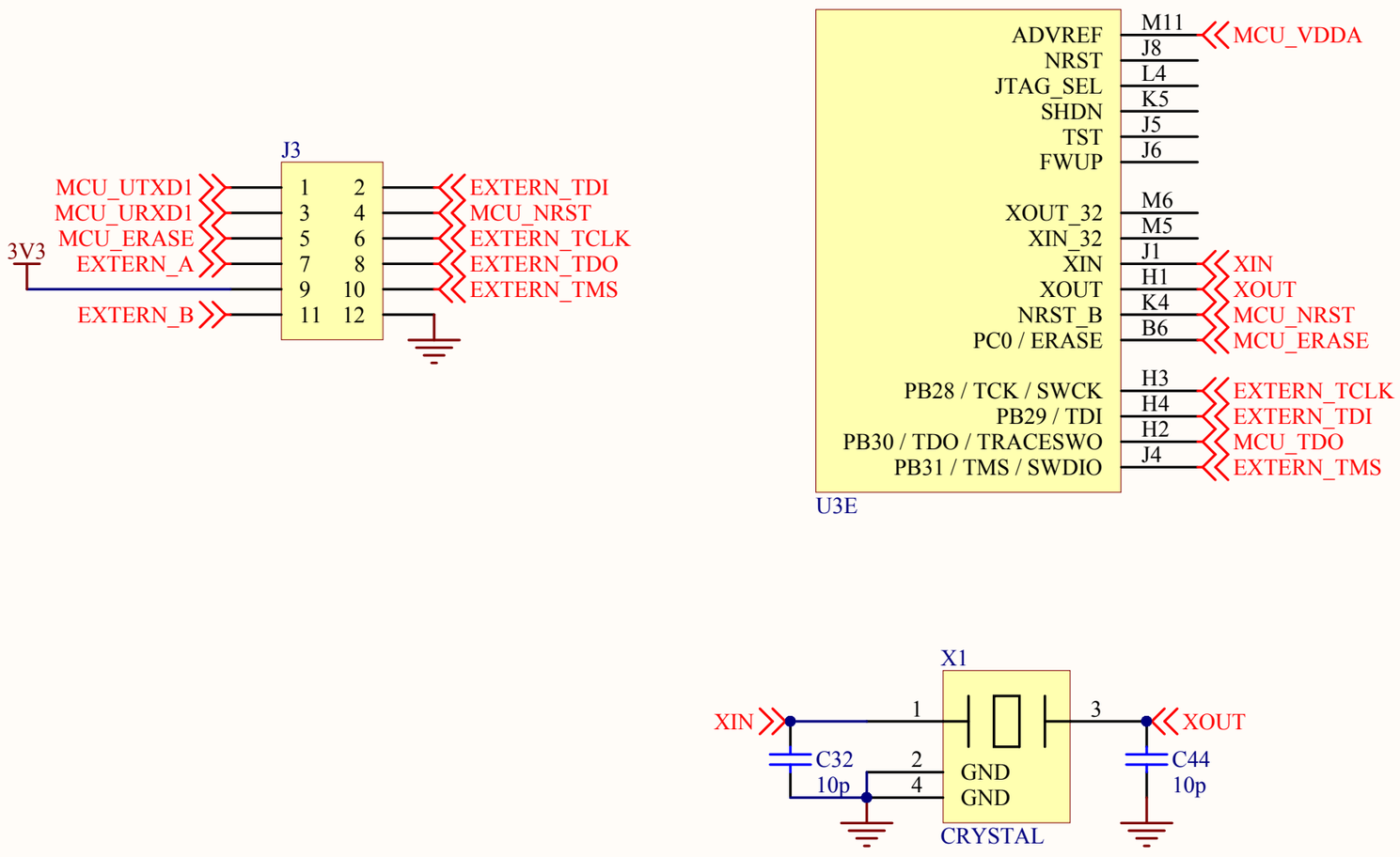
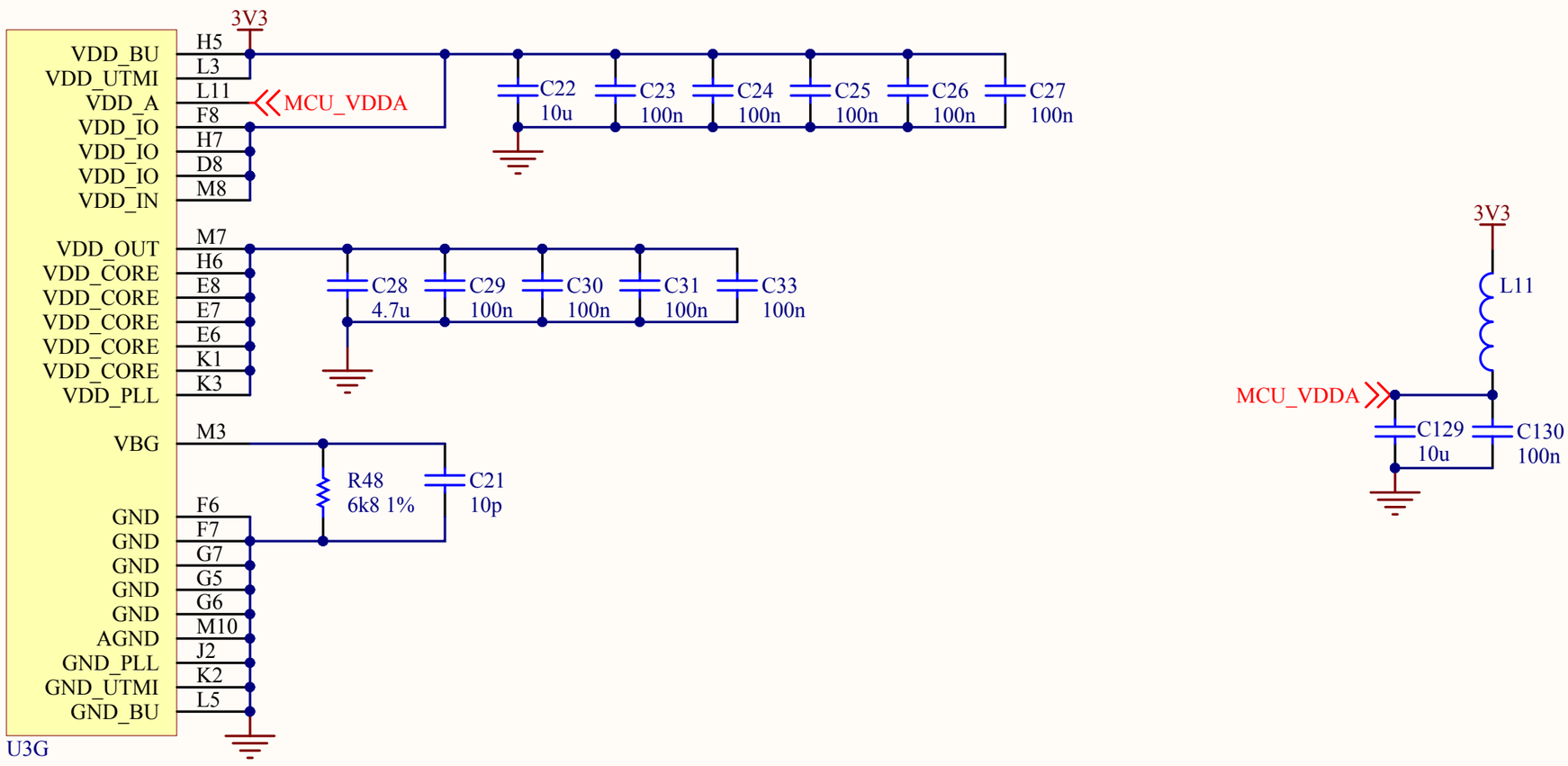


Title *Mobo: MCU I/O*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	Open Source Robotics Foundation
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 4 of 13	
Designer: Morgan Quigley			

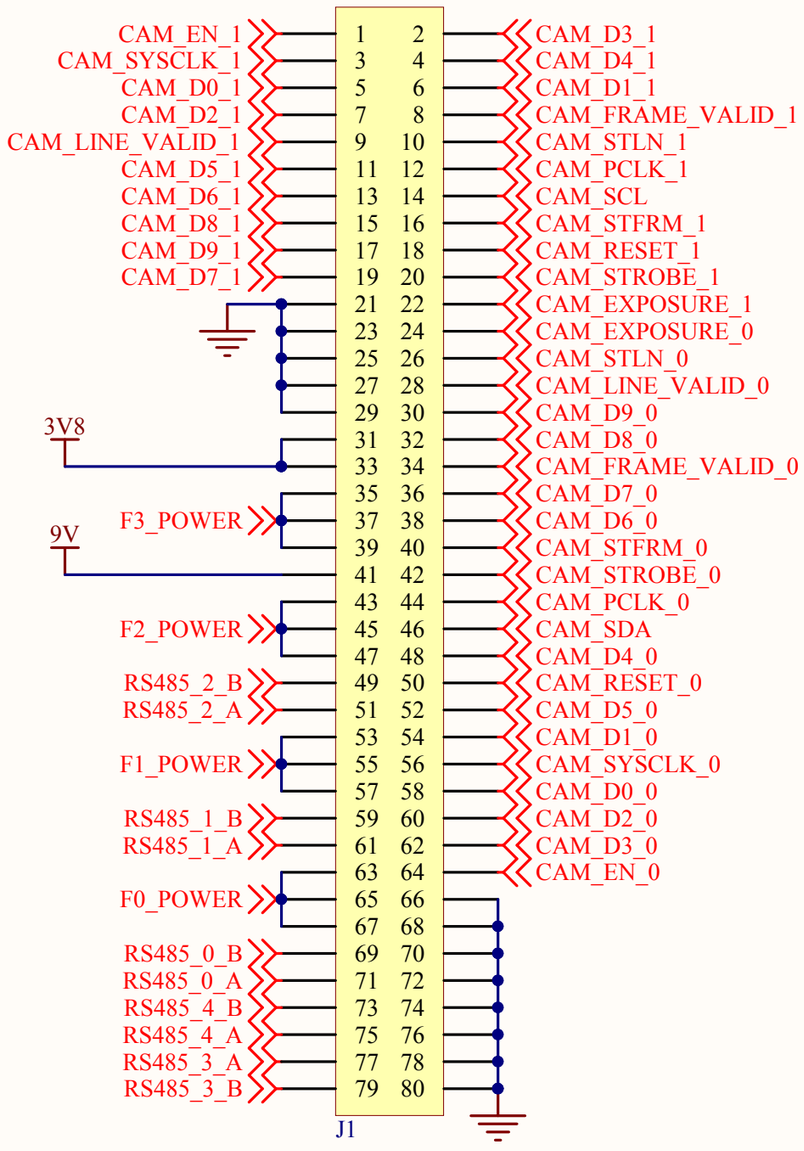


Title *Mobo: MCU Configuration*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 5 of 13	
Designer: Morgan Quigley			

Open Source Robotics Foundation



Title *Mobo: MCU Power*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	Open Source Robotics Foundation
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 6 of 13	
Designer: Morgan Quigley			



4 fingers @ 1.5A = 3 pins * 4 = 12 pwr, 10 gnd

1 pwr, 1 gnd for palm

5 channels rs485 = 10 pins

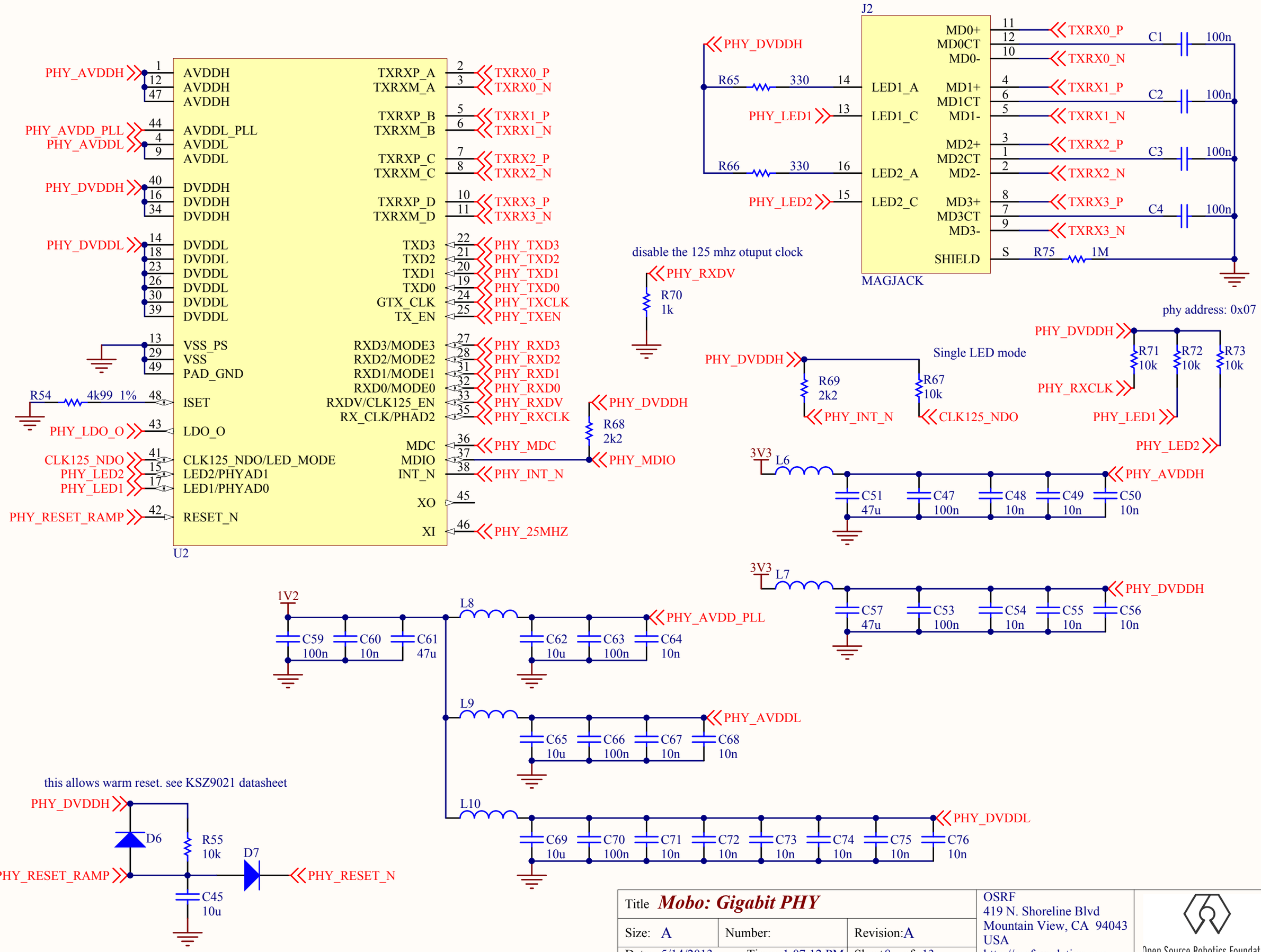
total fingers + palm = 34

21 signals per camera = 42

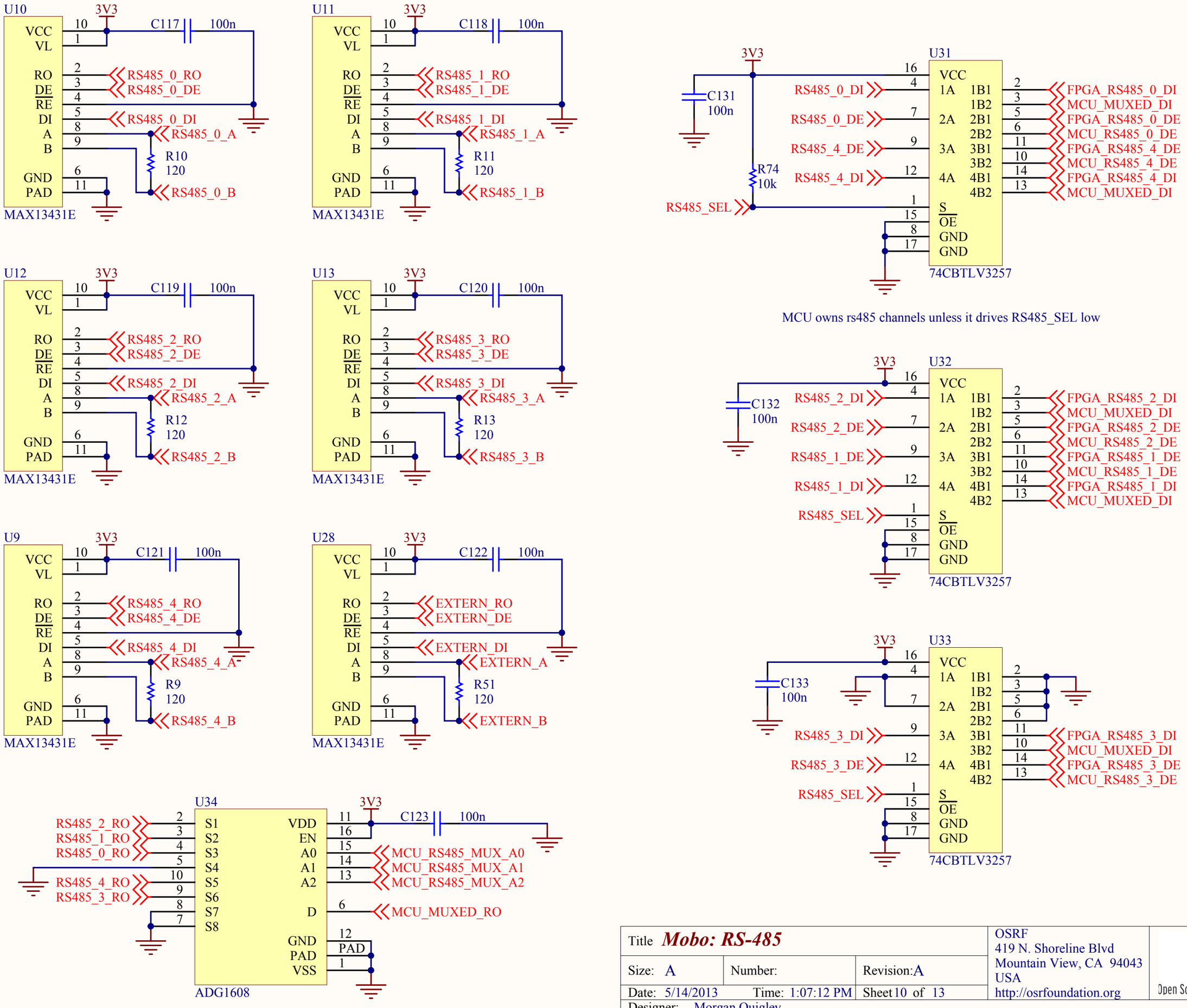
1 power, 1 gnd per camera = 4

total gnd: 10 fingers, 1 palm, 2 cams = 13

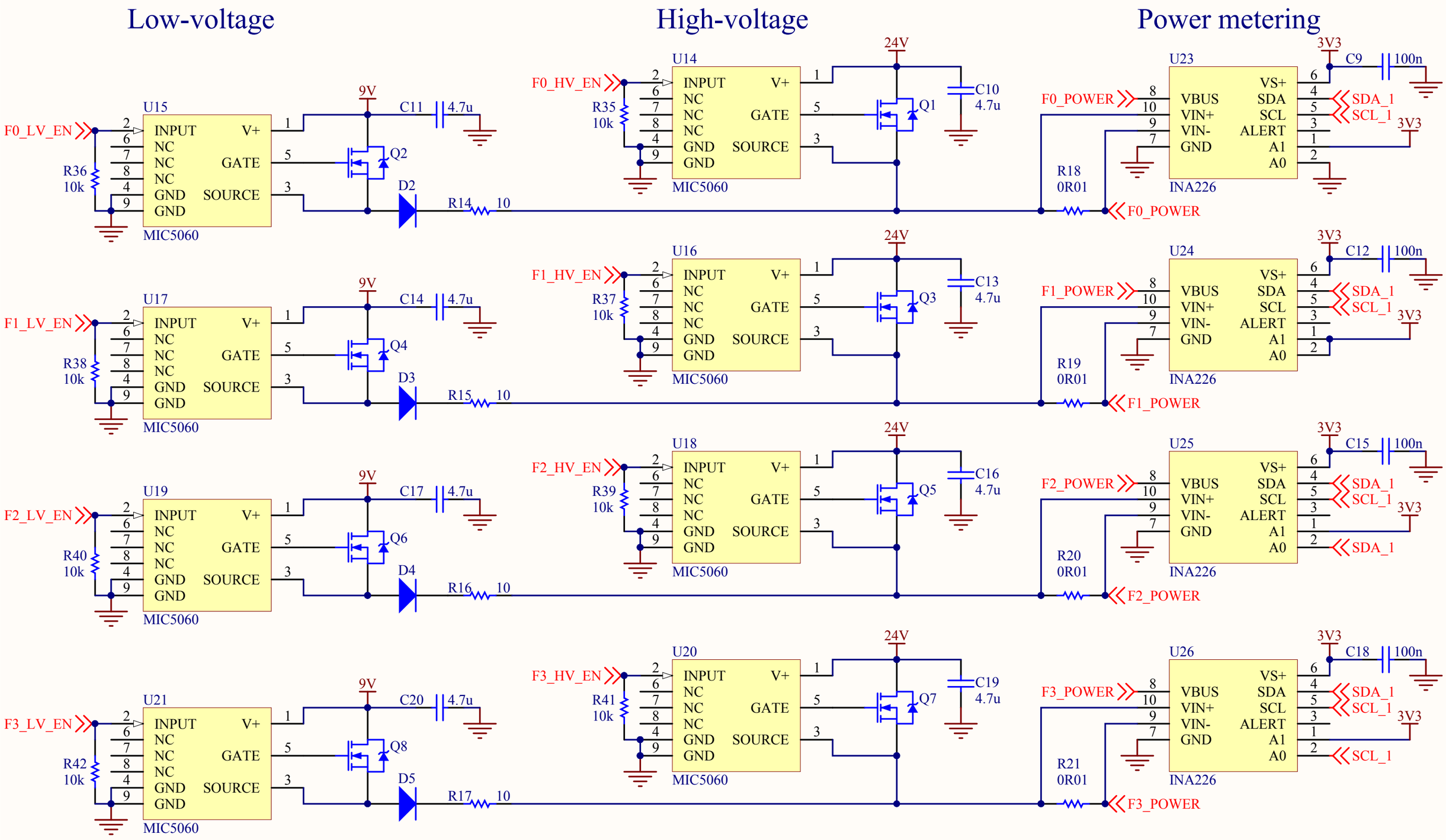
Title ***Mobo: Backplane Connector***			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org Open Source Robotics Foundation
Size: A	Number:	Revision: A	
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 7 of 13	
Designer: Morgan Quigley			



Title *Mobo: Gigabit PHY*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org Open Source Robotics Foundation
Size: A	Number:	Revision: A	
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 8 of 13	
Designer: Morgan Quigley			



Title *Mobo: RS-485*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	Open Source Robotics Foundation
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 10 of 13	
Designer: Morgan Quigley			



Title *Mobo: Finger Socket Switching*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	Open Source Robotics Foundation
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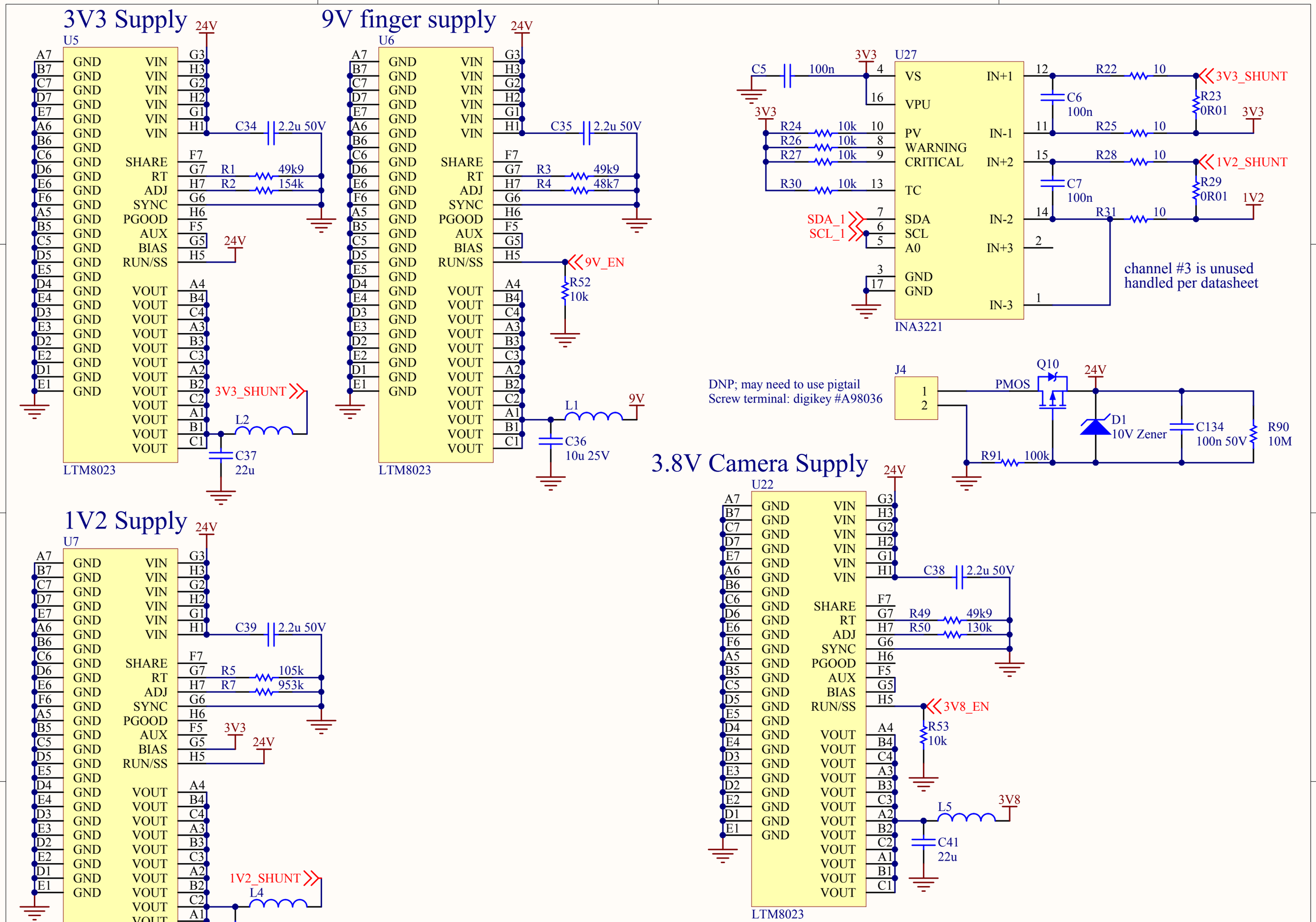
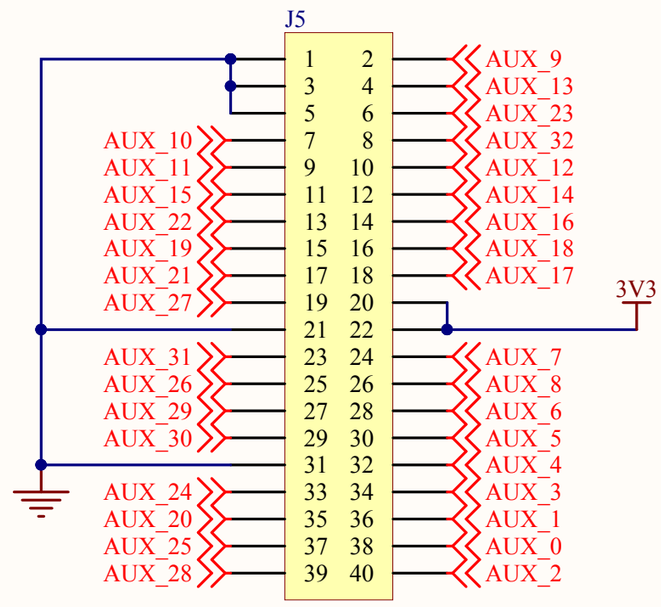
Designer: Morgan Quigley			



Title *Mobo: Power Supplies*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
Size: A	Number:	Revision: A	Open Source Robotics Foundation
Date: 5/14/2013	Time: 1:07:12 PM	Sheet 12 of 13	
Designer: Morgan Quigley			



Title *Mobo: Auxilliary FPGA Connector*			OSRF 419 N. Shoreline Blvd Mountain View, CA 94043 USA http://osrfoundation.org
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Date: 5/14/2013	Time: 1:07:13 PM	Sheet 13 of 13	
Designer: Morgan Quigley			

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